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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,943	03/12/2004	Jong-Joo Lee	25611-000080/US	6887

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EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,943	LEE, JONG-JOO	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Akram et al (U.S. Patent #6028365).

With respect to **claim 12**, Akram teaches providing a first individual package of an area array type (AAT) on a flexible cable (Fig. 4, 226) wherein connecting pads under the AAT package are electrically connected to conductive patterns on the flexible cable (Fig. 4, 237); bending the flexible cable to extend around at least one side edge of the package (Col 9 Ln 35-37); and stacking a second individual AAT package on the first AAT package wherein connecting pads under the second package are electrically connected to the conductive patterns on the flexible cable (Fig. 4, 354).

With respect to **claim 14**, Akram teaches a plurality of external connection terminals under the first package (Fig. 4, 254).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 7, 9, 11, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al (U.S. Patent #6028365), in view of Bai et al (U.S. Patent #6326700).

With respect to **claim 1**, Akram teaches at least two packages of area array type disposed to form a stack (Fig. 4), each package including: a substrate having a first face and a second face opposing a first face (Fig. 4, 330), there being a plurality of terminal pads on the second face (Fig. 4, 337 and 237) and a plurality of connecting pads formed on the first face (Fig. 4, 336 and 236), and a semiconductor chip attached to the first face of the substrate and electrically connected to the terminal pads and the connecting pads (Fig. 4, 220 and 320); and at least one flexible cable having a plurality of conductive patterns thereon extending around at least one side edge of a lower one of the at least two packages, and electrically coupling the connecting pads of the packages through the conductive patterns (Fig. 4, 326), but Akram does not teach that there are a plurality of terminal and connecting pads formed on the second face, and that the chip is formed on the first face. Bai teaches a semiconductor package wherein a

chip (Fig. 1, 20) is attached to a first face of a substrate (Fig. 1, 21) with terminal (Fig. 1, 211a) and connecting pads (Fig. 1, 211b) formed on the second face of the substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the chip, terminal pads, and connecting pads of Akram on the substrate in the configuration taught by Bai in order to reduce the thickness of the package.

With respect to **claim 2**, Akram and Bai teach all of the limitations of claim 1, but Akram does not teach that the semiconductor chip is a center pad chip. Bai teaches a semiconductor chip that is in a center pad configuration (Fig. 1, 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the chip of Akram as a center pad chip as taught by Bai in order to allow the for the profile of the package to be reduced.

With respect to **claim 3**, Akram teaches that the substrate further has first wirings providing electrical paths coupling the semiconductor chip and the terminal pads (Fig. 4, 326 and 226) and second wirings providing electrical paths coupling the semiconductor chip and the connecting pads (Fig. 4, 340 and 240).

With respect to **claim 4**, Akram teaches that the semiconductor chip is an edge pad type chip (Fig. 4, 322).

With respect to **claim 7**, Akram teaches that the connecting pads are arranged in a straight row near an edge of the substrate (Fig. 1A, 22).

With respect to **claim 9**, Akram teaches a plurality of external connection terminals formed on the terminal ads of a lowermost package of the packages (Fig. 4, 254).

With respect to **claim 11**, Akram teaches that each that each area array type package is a ball grid array package (Fig. 4, 354 and 254).

With respect to **claim 16**, Akram teaches that the first wirings are formed on the second face of the substrate (Fig. 4, 326 and 226).

Claims 5, 6, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram and Bai, in view of Taniguchi et al (U.S. Patent #6388333).

With respect to **claims 5 and 6**, Akram and Bai teach all of the limitations of claim 4, and furthermore Akram teaches that the substrate further has first wirings providing electrical paths coupling the chip and the terminal pads (Fig. 4, 326, 226) and second wirings (Fig. 4, 337, 237), but does not teach second wirings including vias providing electrical paths coupling the chip and the connecting pads. Taniguchi teaches wiring including vias (Fig. 6, 9) in immediate proximity to the connecting pads (Fig. 6, 5) coupling the chip and connecting pads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the substrate of Akram with vias as taught by Taniguchi in order to achieve wiring connections using less wiring length.

With respect to **claim 17**, Akram teaches first wirings arranged on the first face of the substrate (Fig. 4, 326, 226), and that the second wirings are arranged on the second face of the substrate (Fig. 4, 237, 337).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akram and Bai, in view of Takashima et al (U.S. Patent #6160313).

With respect to **claim 8**, Akram and Bai teach all of the limitations of claim 1, but do not teach that the connecting pads are arranged in a staggered row near an edge of the substrate. Takashima teaches connecting pads that arranged in a staggered row near an edge of a substrate (Fig. 9, 32C). It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the connecting pads of Akram and Bai in a way as taught by Takashima in order to implement wire bonding with a high accuracy.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akram and Bai, in view of Cady et al (U.S. Patent #6576992).

With respect to **claim 10**, Akram and Bai teach all of the limitations of claim 1, but do not teach a non-conductive adhesive layer interposed between adjacent lower and upper packages. Cady teaches a non-conductive adhesive layer interposed between adjacent lower and upper packages (Fig. 1, 34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to interpose a an adhesive layer between adjacent lower

and upper packages as taught by Cady in order to enhance the mechanical strength of the package.

Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram, in view of Cady.

With respect to **claims 15-17**, Akram teaches providing a first package of an area array type (AAT) on a flexible cable (Fig. 4, 326) wherein connecting pads (Fig. 4, 337) under the package are electrically connected to conductive patterns on the flexible cable; attaching a second AAT package to the first package; and bending (Col 9 Ln 35-37) the flexible cable to extend around at least one side edge of the second AAT package wherein connecting pads under the second package are electrically connected to the conductive patterns on the flexible cable (Fig. 4, 237), but does not teach forming an adhesive layer under the first package and attaching the two packages together by the adhesive layer. Cady teaches a non-conductive adhesive layer interposed between adjacent lower and upper packages (Fig. 1, 34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to interpose a an adhesive layer between adjacent lower and upper packages as taught by Cady in order to enhance the mechanical strength of the package.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
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